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EXAMINER	
SELLMAN, CACHET I	
ART UNIT	**PAPER NUMBER**
1762	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,473	PARK, SANG KYUN	
	Examiner	Art Unit	
	Cachet I. Sellman	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4-13 and 17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-13 and 17-19* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-18-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-3 and 14-16, drawn to an apparatus, classified in class 438, subclass 1+.

II. Claims 4-13 and 17-19, drawn to a process, classified in class 427, subclass 523.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the apparatus can be used in a materially different process such as forming metal wires on a substrate other than silicon or one that does not form both lower and upper metal wires.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with James Zeller on October 19, 2005 a provisional election was made with traverse to prosecute the invention of Group II, claims 4-13 and 17-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-3 and 14-16 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

6. The abstract of the disclosure is objected to because it contains legal terminology and minor informalities.

- The applicant uses the word "disclosed" in the abstract.
- Line 3 of the abstract states "sheet for forming metal wires" and line 4 states "plate for forming the metal wires".

Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities: The disclosure is objected to because of the following informalities: On page 8 line 23 of the specification there seems to be a typographical error "an in Fig 2" should read "as in Fig 2".

Appropriate correction is required.

Drawings

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character:

- "105" has been used to designate both "copper film" (pg 2, line 2 and "copper wires" (pg2, line 4).
- "112" has been designated both "copper film" (pg 2, line 21) and "copper wires" (pg 3, line 3)

9. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- Page 2 line 22 of the specification references "the trench 110" and "the via hole 108" of Figure 10 but they are not labeled in the drawing.

- Page 3, line 3 of the specification references "via hole 108" of Figure 1D but it is not labeled in the drawing.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

10. Claims 4 and 17 are objected to because of the following informalities: Claims 4 and 17 reads "adhering a plate having a plate in which a plurality" it should read "adhering a plate in which a plurality". Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant requires "a compound of Ni, Co, P and B" it is not clear if the applicant is claiming a compound that consists of Ni, Co, P, and B or a compound that contains Ni, Co, P or B.

13. Claim 19 recites the limitation "the annealing processes in the steps d and e" in the first and second lines of claim 19. The applicant references an annealing step of claim 17 in steps d and e but in claim 17 the applicant does not provide an annealing step. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Hofmann (US 6716754 B2).

Hofmann teaches a method for forming patterns in low-k dielectric materials by using a mold in contact lithography (abstract). A semiconductor construction consists of a substrate and contact pads and a low-k dielectric material (such as a low k polymer) (column 4, lines 5-15 and figure 2). A mold having a patterned surface comprising projections and valleys between the projections (column 4, lines 16-38 and figure 3) is pressed together with the semiconductor construction to implant the low dielectric material within the mold and once the mold is removed a pattern is formed within the low-k material (column 4, lines 40-51, and figure 4). The low-k dielectric layer has a pattern in which openings are extending through and the contact pads are exposed within the openings (figure 5). The patterned material contains both shallow trenches and deep openings (column 5, lines 12-15 and figure 6). Hofman teaches that various chemical and/or plasma cleaning steps can be introduced to insure that the conductive material (contact pads) is well exposed (column 4, lines 64-67). A conductive material, which comprises one or more metal such as copper, aluminum, tungsten or titanium, is formed over the patterned dielectric layer (column 5, lines 6-10 and figure 6). The conductive material and dielectric layer are both subjected to chemical-mechanical polishing (column 5, lines 19-20). An insulative layer is formed over the conductive wires (column 5, lines 36-39). Hofmann further teaches that another mold can be placed over the second insulative layer to form another pattern comprising of openings extending through

the redistribution layer s (figure 10); then conductive material is formed across the insulative layer within the openings (figure 11) as required by **claim 17**.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 4-5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman (US 6716754 B2) in view of Chen et al. (US 585869).

Hoffman teaches a method for forming a semiconductor construction where a low dielectric material, which can comprise Cyclotene, is formed on a silicon substrate then trenches are formed in the low dielectric material using contact lithography and a conductive material is formed above the patterned low dielectric material forming lower metal wires (figures 2-7). Another layer of low dielectric material is formed above the lower metal wires then a mold having a patterned surface comprising projections and valleys between the projections (column 4, lines 16-38 and figure 3) is pressed together with the semiconductor construction to implant the low dielectric material within the mold and once the mold is removed a pattern is formed within the low-k material (column 4, lines 40-51, and figure 4). The low-k dielectric layer contains both shallow trenches and deep openings (column 5, lines 12-15 and figure 6). Upper metal wires are formed which are connected to the lower metal wires through the via holes (figure 11).

Hoffman does not teach annealing the low-dielectric material as required by **claim 4**.

Chen et al. teaches a method for making multilevel electrical interconnections with a low dielectric constant material such as a organic materials, polysilsequioxane (Si polymer), benzocyclobutene (Cyclotene) or a fluorinated polyimide (column 6, lines 16-20), in which a low dielectric constant insulator is annealed at a temperature between 80°C-450°C to cure the organic insulator (column 6, lines 23-25).

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process taught by Hofman to include the step of annealing the low dielectric material of Chen et al. One would have been motivated to do so because both Hofman and Chen et al. teach processes for forming multilevel interconnect structures using Cyclotene therefore one would have a reasonable expectation of success in forming the interconnect structure with a cured insulator.

Chen et al. teaches using a barrier layer prevents penetration of the metal into other layers (column 5, lines 35-39) as required by **claims 5 and 10**. As stated above the temperature of the mold and the substrate is between 80°C – 450°C as required by **claim 7**. The low dielectric material can be an organic material, polysilsequioxane, or benzocylcobutene, and have a thickness between 2000 and 20000 Angstroms (column 6, lines 16-20) as required by **claim 8**. Chen et al. further teaches that the annealing step can take form 0.5 to 2 minutes as required by **claim 9**.

18. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (US 6100184), in view of Hofmann (US 6716754 B2).

Zhao et al. teaches a method for making an interconnect structure using low dielectric constant material. In the method taught by Zhao et al. a low dielectric material is formed on a silicon wafer then a trench is formed and a metal is formed within the trench (column 4, lines 15-25 and figure 1). Another layer of low dielectric material is formed over the conductive layer then dielectric layer is patterned using a photolithography technique; next a dielectric barrier layer is formed then another low dielectric layer is formed and is patterned using photolithography technique (figures 3-9, column 6, lines 10-67). A

conductive material is then placed in the via hole therefore forming upper wires that are connected to lower metal wires.

Zhao et al. does not teach using a plate with an engraved pattern for forming a plurality of trenches and via holes onto the silicon substrate as required by **claim 17**.

Hofmann discloses a method for forming patterns in low dielectric materials using contact lithography, where a mold having a pattern is pressed into a low dielectric material (abstract). Hofman teaches that there are numerous difficulties in forming appropriate openings in the insulative material for the redistribution layer as well as the conductive materials but by using the mold to form the pattern will alleviate or eliminate these problems (column 2, lines 12-17). Hofman further teaches that using contact lithography is advantageous because it can be faster and cheaper than other patterning methods such as photolithographic methods (column 5, lines 29-33).

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for making a dual damascene interconnect structure taught by Zhao et al. to include using the mold of Hofmann to form vias and trenches in the low dielectric materials. One would have been motivated to do so because both Zhao et al. and Hofmann teach processes for forming semiconductor integrated circuits and Hofman teaches that using the mold to form the patterned semiconductor component is faster and cheaper than photolithographic methods therefore one would have a reasonable expectation of success in forming the semiconductor component at a faster rate and a lower cost.

Hofman further teaches that low dielectric materials are those that have a dielectric constant below 3.5 (column 1, lines 52-55). Zhao et al. further teaches that chemical-mechanical polishing is used to polish away the excess conductive material above the trench level and the dielectric layer functions as a polish-stop layer (column 8, lines 56-60; figure 11) as required by **claim 18**.

19. Claims 4-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al in view of Hofmann as applied to claims 17 and 18 above, and further in view of Venkatraman et al. (US 2003/0141499 A1).

Zhao et al. in view of Hofmann teaches a process for forming a dual damascene structure using a low dielectric material and contact lithography where a mold is used to form trenches and vias in the dielectric film as mentioned above.

Zhao et al. in view of Hofmann does not teach annealing the insulating materials as required by **claims 4 and 19**.

Venkatraman et al. teaches a process for depositing low dielectric constants and in the process it states that after depositing the low dielectric material it can be annealed to further lower the dielectric constant. Venkatraman et al. further teaches that the annealing must be performed in an inert gas environment, at either atmospheric pressure or under vacuum. Venkatraman et al. further teaches that annealing times vary from 1 minute to 10 hours and the temperature is in the range of 100°C to 500°C.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for forming a dual damascene structure taught by Zhao et al. in view of Hofmann to include the annealing step of Venkatraman et al. in order to form an insulating layer with a low dielectric constant. One would have been motivated to do so because both Zhao et al. in view of Hofmann and Venkatraman et al. teach the use of materials which contain carbon, hydrogen, silicon and oxygen as the low dielectric material therefore one would have a reasonable expectation of success in forming the dual damascene structure with a low dielectric constant material.

Zhao et al. further teaches that a barrier layer is sued to inhibit or prevent copper diffusion into the dielectric layer (column 5, lines 17-19) as required by **claims 5 and 10**. The barrier layer can be formed

from cobalt tungsten phosphide using selective electroless deposition (column 10, lines 22-26) as required by **claim 6.** The barrier layer can also be formed of TiN, Ta, TaN, W, WN, SIN, and WSiN (column 5, lines 23-24) using chemical vapor deposition (column 6, line 1) as required by **claims 12 and 13**. As stated above the annealing step is performed at a temperature between 100°C– 500°C and for 1min - 10 hours as required by claims **7 and 9**. The low dielectric material used can be organic materials (polyimides or polymers) or modified SiO2 materials (fluorinated oxide or silsesquioxane) (column 2, lines 2-7) and is deposited with an approximate thickness of 500-10000 Angstroms (column 6, lines 20-22) as required by **claim 8**. Zhao et al. teaches that the upper and lower wires can consist of a barrier film and copper film and is formed using a damascene process (Figures 14-16) as required by **claim 11**.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cachet I. Sellman whose telephone number is 571-272-0691. The examiner can normally be reached on Monday through Friday, 7:00 - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TIMOTHY MEEKS
SUPERVISORY PATENT EXAMINER

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Art Unit 1762